(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 622 733 A1**

(12) **EUROPEAN PATENT APPLICATION**

(21) Application number: **93830186.8**

(51) Int. Cl.5: **G06F 11/00**, G01R 31/28

(22) Date of filing: **30.04.93**

(43) Date of publication of application: **02.11.94 Bulletin 94/44**

(84) Designated Contracting States: **DE FR GB IT**

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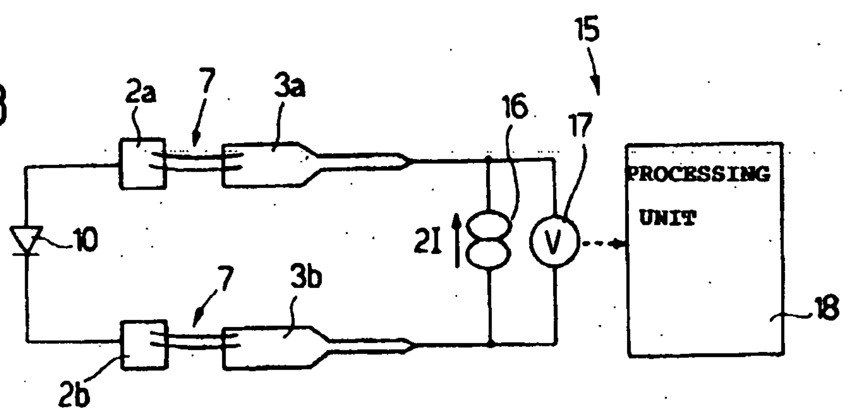
(54) Method and device for testing integrated power devices.

(57) A test method whereby a high current is supplied to a first pin (3a) of an integrated device to be tested, and the variation in the voltage drop between the first pin and a second pin (3b) on the device to be tested is determined; the two pins being connected to two pads (2a, 2b) in turn connected, inside the device to be tested, by a low-voltage-drop path (10). The variation in the voltage drop of the device to be tested is compared with the measured nominal variation of an undoubtedly sound device of the same type, to determine any excessive deviation indicative of deficiency. The supply current in fact results in power dissipation, local heating and, consequently, a variation in the resistance of the connecting wires or of the die attachment to the lead frame, the extent of which differs according to whether only one or both of the wires (8) of a two-wire connection (7) to be tested are present, and according to whether the die is attached properly, poorly or badly to the lead frame. This variation in resistance is reflected in the amount or speed by which the detected voltage drop varies, thus enabling sound parts to be distinguished from faulty ones.

FIG. 3



EP 0 622 733 A1

The present invention relates to a method and device for testing integrated power devices.

As known, on integrated power devices, each contact pad on the device is connected to a respective pin on the lead frame using two parallel wires, so as to increase the maximum current withstandable by the connection. A 2 mil gold wire, for example, is incapable of withstanding indefinitely a current of over 2 A, so a second wire is added parallel to the first to double the current capacity.

The problem therefore arises of automatically testing the integrity and correct bonding of both the wires, in view of the bonding process currently employed involving a deficiency rate of roughly 50-100 ppm. Traditional test methods, however, such as measuring pin-to-pin continuity, fail to provide for discriminating between a faulty connection in which only one wire (of a two-wire connection) is present, and correct connection of both wires, in that the resistance of gold wires is negligible as compared with the overall resistance of the circuit under test. For example, a 2 mil, 3 mm long gold wire presents a resistance of 33 mΩ. Assuming the test is conducted using 1 A current, the voltage drop will be 33 mV, which is roughly a hundred times smaller than the voltage drop (roughly 3 V) on the series diode normally provided. Bearing in mind dispersion of the voltage drop on the diode, the different voltage drop due to the presence of one as opposed to two wires is thus undetectable.

One known solution to the above problem consists in providing two contact pads connected by a respective wire to the same pin. While enabling testing in the conventional way, such a solution involves an increase in the area of the device, due to the greater number of contact pads employed, which, in view of the current tendency towards ever increasing miniaturisation of integrated circuits and devices, is strictly undesirable.

Moreover, on power devices, the necessity frequently arises of testing attachment of the die to the lead frame in the areas involving the power elements of the circuit (typically the final power stages) for ensuring adequate power dissipation.

It is an object of the present invention to provide a test method designed to overcome the drawbacks typically associated with known methods.

According to the present invention, there is provided a method of testing integrated power devices, as claimed in Claim 1.

The present invention also relates to a device for testing integrated power devices, as claimed in Claim 9.

A preferred, non-limiting embodiment of the present invention will be described by way of example with reference to the accompanying drawings, in which:

Fig.1 shows a view in perspective of two two-wire connections between two contact pads of an integrated power device and respective pins;

Fig.2 shows a graph of electrical quantities employed in the method according to the present invention;

Fig.3 shows a circuit diagram of the test device according to the present invention, for testing the two-wire connections in Fig.1;

Fig.4 shows a flow chart of one embodiment of the method according to the present invention;

Fig.5 shows the electric diagram of a portion of an integrated device to which the present method is applied.

Fig.1 shows a portion of an integrated device 1 of which the connections between contact pads 2a, 2b and respective pins 3a, 3b are to be tested. The die 4 of device 1 is fixed to lead frame 6 by a known bonding layer 5, and pads 2 are connected to respective pins 3 by respective two-wire connections 7, each consisting of two parallel gold wires 8.

The method according to the present invention is based on the fact that, when a two-wire connection is supplied with fairly high current, a considerable amount of power is dissipated by the wires, which are thus heated. Consequently, as the resistance of gold wires depends closely on temperature, by monitoring the voltage drop produced by the current as a function of time, it is possible to distinguish between two-wire connections and faulty ones, in which only one of the two wires has been correctly bonded. In fact, with the same current supply, if only one wire is present, all the current will flow through this, thus resulting in four times the power dissipation of a correct connection, in which the current is divided substantially equally between the two wires. In the event of a faulty connection, therefore, this will result in a greater increase in the temperature, in a greater increase in the resistance and, hence, in a higher voltage drop of the wire, so that, by comparing the voltage drop as a function of time with that of the same connection on a part known to be sound, it is possible to determine the absence of one of the wires.

Moreover, monitoring the voltage drop produced by a high current supply also provides for testing attachment of the die to the lead frame in the areas involving the power elements of the circuit. Poor attachment in fact (air pockets between the corresponding die region and the lead frame) results in a more rapid increase in die-lead frame thermal resistance and, hence, in a change in thermal behaviour. As such, parts with poorly attached dies may be detected by measuring the speed at which the voltage drop varies over a predetermined time period after the high current is applied, and by comparing this with a standard (correct) value. In

this case, the pads need not necessarily be two-wire-connected to the pin, the only requirement being that it be an integrated power device with a good degree of power dissipation through the lead frame, and to which, among other things, a high current may be supplied for adequately differentiating between the behaviour of parts with correctly, poorly, or badly attached dies.

By way of explanation, the Fig.2 graph shows the normalized voltage drop DV with respect to the value measured at the start instant, i.e. by subtracting from the value measured at each instant the initial voltage drop value measured immediately following application of the current. In particular, the curves show the normalized voltage drop DV resulting from supplying a constant high current between two pins two-wire-connected to respective pads in turn mutually connected by a diode. Fig.2 shows four curves relative to experimental measurements conducted on four theoretically identical parts, but with different problems as regards wire connection or die attachment. Curve A shows the results of a series of measurements relative to a part presenting both the two-wire connections and a correctly attached die; curve B to a part presenting the two-wire connections but a poorly attached die; curve C to a part lacking one of the wires on one of the connections; and curve D to a part presenting the two-wire connections but a badly attached die. As can be seen, in the event of a disconnected wire or badly attached die (curves C and D), after a given time interval, e.g. 40-50 ms, voltage drop DV is considerably greater than that of a perfectly sound part (curve A) or one with a poor, though still acceptable, die attachment (curve B). On the basis of the above information alone, therefore, it is possible to distinguish between sound and defective parts. In addition, however, it is possible to determine whether the problems involved are due to the absence of one of the wires or to a badly attached die by evaluating the voltage drop over the final portion of the measurement. In fact, over the final portion, curve D relative to a badly attached die presents twice the slope of curve C relative solely to the absence of one wire, so that each may be distinguished by simply monitoring DV over the final portion of the measurement.

One embodiment of the test device and method according to the present invention will now be described with reference to Fig.s 3 and 4.

Fig.3 shows the electric diagram of device 1 in Fig.1, wherein pads 2a and 2b are assumed mutually connected by a diode 10. Pins 3a and 3b are connected to the test device indicated by 15 and including a current source 16 series connected between pins 2a and 2b; a voltage measuring element 17 parallel to source 16; and a processing unit 18, which may, of course, incorporate voltage measuring element 17. When a current 2I is supplied by source 16, therefore, in the event each connection 7 presents both wires 8, each wire 8 will be supplied with current I, thus resulting in current dissipation of RI^2, where R is the resistance of the wire (variable as a function of time). Conversely, if one of the wires of even only one of connections 7 is absent, the remaining wire in the same connection is supplied with the whole of current 2I, thus resulting in current dissipation of $4RI^2$, that is, four times the dissipation of a correct connection. The wire of the one-wire connection therefore presents a higher temperature and produces a more rapidly increasing voltage drop as compared with the part with a correct (two-wire) connection.

The method according to the present invention therefore consists initially in measuring and memorizing data relative to undoubtedly sound parts, i.e. having both two-wire connections and a good die attachment. For this purpose, a high current is supplied (by which is meant a current high enough to cause an evident variation in the thermal resistance of the wire and in the die attachment, e.g. 5 A), and the resulting normalized voltage drop is measured, for example, by sampling it at successive instants. Voltage drop $DV_T(t)$ is thus determined at a given instant t_2 (e.g. after 50 ms), and a quantity is calculated correlated to the slope of the curve at the final step, e.g. the difference dV_T between the DV values measured at two successive instants t_1 and t_2 according to the equation:

$$dV_T = DV_T(t_2) - DV_T(t_1).$$

This step is indicated in Fig.4 by block 25.

The same high current is then supplied to the device for testing (block 26), and the corresponding DV values at instant t_3, and the difference $dV = DV(t_2) - DV(t_1)$ between DV at instants t_2 and t_1 are measured (block 27).

The correct values $DV_T(t_2)$, dV_T are then compared in block 28 with the test values $DV(t_2)$, dV, and, in the event the difference between even one of the test values and the respective nominal value exceeds a predetermined value K_1, K_2 (YES output of block 28), the part is rejected (block 29). Conversely, the test is terminated. Values K_1, K_2 are conveniently determined on the basis of deviation σ of a group of undoubtedly sound devices (e.g. $K_1 = K_2 = 6\sigma$).

The Fig.4 process is obviously repeated for all the two-wire connections for testing, or at any rate for all the connections with power regions whose die attachment is to be tested.

The advantages of the method and device according to the present invention will be clear from

the foregoing description. In particular, they provide for safely detecting the absence of even only one wire in a two-wire connection, thus ensuring top quality and reliability of the passed devices, and with no increase in the area of the device as a result of doubling the power contact pads.

Moreover, the solution described is highly straightforward, requires no complicated hardware, and provides for extremely high-speed testing in 30-50 ms.

Finally, as already stated, in addition to determining the presence of both wires in two-wire connections, the method and device described also provide for simultaneously testing die attachment in the power elements (output power stages).

To those skilled in the art it will be clear that changes may be made to the method and device described and illustrated herein without, however, departing from the scope of the present invention. In particular, the present method may be applied to any pair of power pins, providing the respective pads are mutually connected by a low-voltage path, and especially when the voltage drop produced by the internal path is normally no more than 4-5 V.

Generally speaking, the method described does not apply to testing two-wire connections towards the lead frame, as on the emitter of bottom NPN transistors of audio power devices, in which case, as opposed to flowing through the two-wire connection and the pad, the current flows through the substrate, as shown in Fig.5, which shows the final stage 35 of an audio power device. The Fig.5 example shows a substrate indicated by line 36 and connected to a portion 37 of the lead frame; a supply line 38 connected to a pad 39; a diode 40 interposed between lines 36 and 38; and two final power transistors - PNP transistor 41 and NPN transistor 42 - series connected between lines 38 and 36.

More specifically, transistor 41 is connected by the emitter to supply line 38 and by the collector to pad 43, which is also connected to the collector of transistor 42, the emitter of which is in turn connected to pad 44. A diode 45 is interposed between substrate 36 and pad 43, with its anode connected to (or formed directly by) substrate 36. A diode 46 is interposed between the collector and emitter of transistor 42 (with the anode connected to the emitter); and pads 39, 43 and 44 are connected respectively by a two-wire connection 7 to pins 49, 50 and frame 37.

Assuming to begin with that diode 46 is absent (a reasonable assumption in the great majority of cases), to test the two-wire connection 7 between frame portion 37 and pad 44, it is not enough to supply current to frame portion 37 and measure the voltage drop between this and, say, pin 50, as, in this case, the current would follow the path indicated by the double dotted line 53, and would flow directly from frame portion 37 to substrate 36 and through diode 45 and pad 43 to pin 50. To solve this problem, we propose to specifically provide for diode 46 between pads 43 and 44, and preferably of the same size as pad 44, so as to enable the current to flow from frame portion 37 through two-wire connection 7 to pad 44, and through diode 46 and pad 43 to pin 50, and so enable the voltage drop produced by the current to be measured as described above. In view of the size and location of the special diode provided, such a solution would provide for also testing the two-wire connection towards the lead frame with no increase in the area of the device.

As already stated, the present method and device may also be applied to power devices not featuring two-wire connections, for merely testing the die attachment, providing obviously that the pad-pin connections are capable of withstanding high current (a few Amps).

Finally, the present method may be employed in dual mode, by applying a voltage of a given value or pattern, monitoring the current pattern produced by the thermal resistance of the wires or the die-lead frame attachment, and comparing it with correct values for detecting faulty devices.

Claims

1. A method of testing integrated power devices having contact pads (2a, 2b) connected by power connections (7) to respective pins (3a, 3b); characterized by the fact that it comprises the steps of supplying a first electric quantity between two pins (3a, 3b) of the integrated device (1) to be tested, the two pins (3a, 3b) being connected to two pads (2a, 2b) connected, inside the integrated device (1) to be tested, by a low-voltage-drop path (10); determining the variation in time of a second electric quantity correlated to the first electric quantity by the power dissipation produced by said first electric quantity; and comparing said variation in time with a predetermined nominal variation.

2. A method as claimed in Claim 1, characterized by the fact that said first electric quantity is a high current, and said second electric quantity is the voltage drop between said pins (3a, 3b).

3. A method as claimed in Claim 2, characterized by the fact that said current presents a constant value.

4. A method as claimed in Claim 2 or 3, for determining the absence of a wire (8) in a two-

wire connection (7) between a pin (3a, 3b) and pad (2a, 2b); characterized by the fact that said step of determining said variation in time comprises the step of measuring the voltage between said pins (3a, 3b) after a predetermined time interval from when said current is supplied.

5. A method as claimed in one of the foregoing Claims from 2 to 4, for detecting poor attachment of the die (4) of the integrated device to the lead frame (6); characterized by the fact that said step of determining said variation comprises the step of determining the slope of the curve of said voltage drop in a predetermined time interval.

6. A method as claimed in Claim 5, characterized by the fact that said step of determining said slope comprises the steps of measuring said voltage drop at two successive instants, and determining the difference between the values measured at said two successive instants.

7. A method as claimed in any one of the foregoing Claims, characterized by the fact that it comprises the step of determining said predetermined nominal variation on the basis of at least one reference integrated device identical to the integrated device (1) to be tested and presenting undoubtedly correct connections (7) and/or die attachment; and memorizing said predetermined nominal variation.

8. A method as claimed in Claim 7, characterized by the fact that said step of determining said predetermined nominal variation comprises the steps of supplying said high current to a first pin on said reference integrated device corresponding to said first pin on said integrated device to be tested; and determining the variation in time of said voltage-drop-correlated quantity of said reference integrated device.

9. A device (15) for testing integrated power devices (1) having contact pads (2a, 2b) connected by power connections (7) to respective pins (3a, 3b); characterized by the fact that it comprises: source means (16) for a first electric quantity, connectable between two pins (3a, 3b) of the integrated device (1) to be tested, the two pins (3a, 3b) being connected to two pads (2a, 2b) connected, inside the integrated device (1) to be tested, by a low-voltage-drop path (10); measuring means (17) for determining the variation in time of a second electric quantity correlated with said first electric quantity by the power dissipation produced by said first electric quantity; and comparing means (18) for comparing said determined variation with a predetermined nominal variation.

10. A device as claimed in Claim 9, characterized by the fact that said source means comprise a constant current source (16); and by the fact that said measuring means (17) comprise means for measuring the variation in time of a quantity correlated with the voltage drop between said two pins (3a, 3b).

11. A device as claimed in Claim 10, characterized by the fact that said measuring means comprise a voltage measuring element (17) for detecting the voltage between said pins (3a, 3b) following a predetermined time interval from when said current is supplied.

12. A device as claimed in Claim 10 or 11, characterized by the fact that said measuring means comprise an element (27) for determining the difference between voltage drop values measured at two successive instants.

13. A device as claimed in any one of the foregoing Claims from 10 to 12, characterized by the fact that it comprises means (25) for determining said predetermined nominal variation on the basis of at least one reference integrated device identical to said integrated device (1) to be tested and presenting undoubtedly correct connections and/or die attachment; and memory means for memorizing said predetermined nominal variation.

14. An integrated device (35) testable using the method as claimed in one of the foregoing Claims from 1 to 6; characterized by the fact that it presents a test diode (46) interposed between a power contact pad (43) and a contact pad (44) connected to a substrate (36); said test diode (46) presenting the same area as one of said contact pads (43; 44).

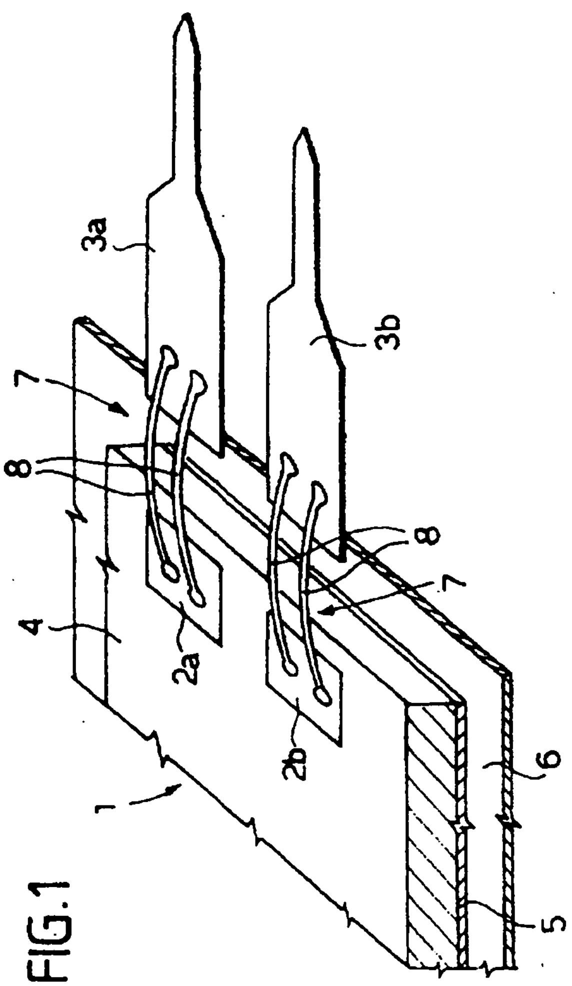


FIG.1

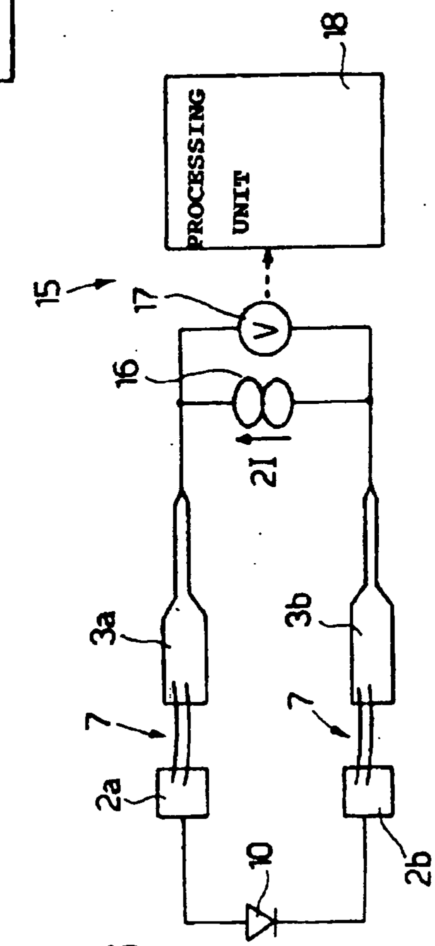


FIG.3

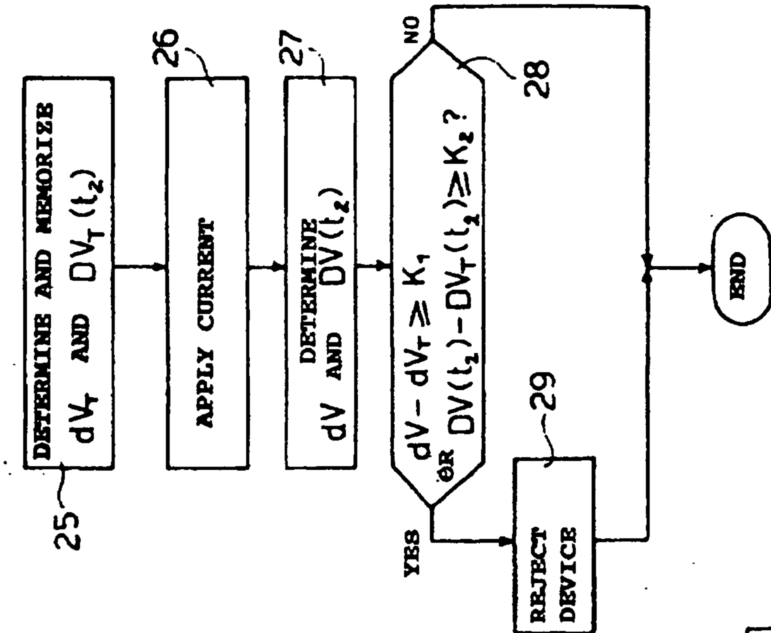


FIG. 4

FIG. 2

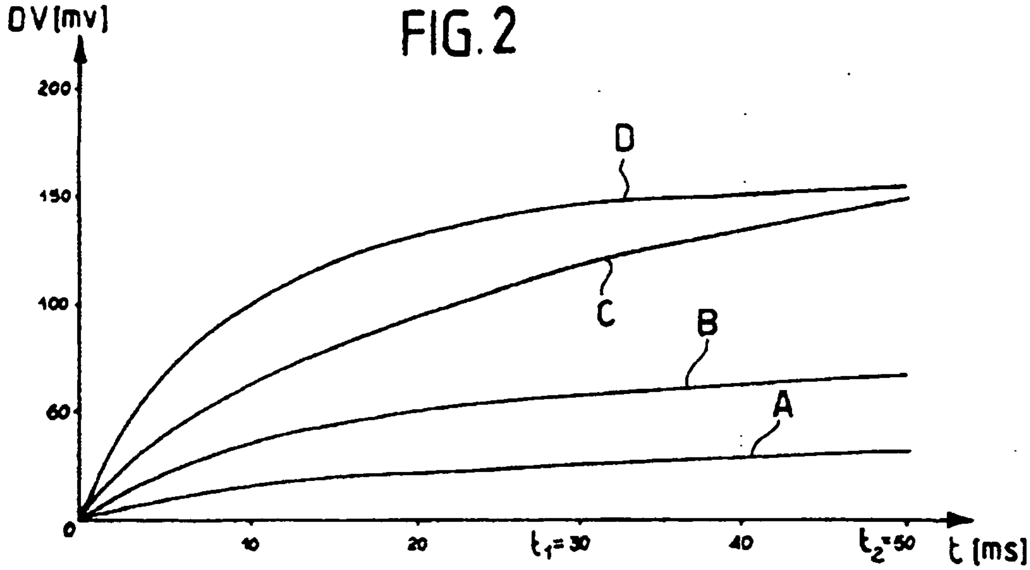

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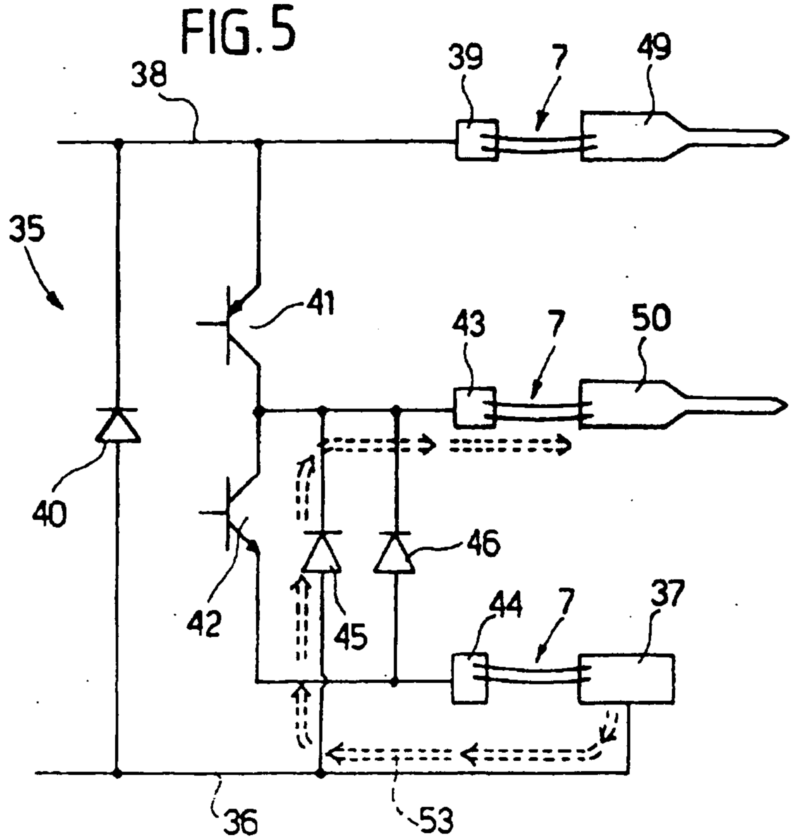
FIG. 5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EUROPEAN SEARCH REPORT

Application Number

EP 93 83 0186

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 075 079 (IBM) ---		G06F11/00 G01R31/28
A	EP-A-0 351 911 (PHILIPS) -----		
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			G01R

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	14 SEPTEMBER 1993	HOORNAERT W.

CATEGORY OF CITED DOCUMENTS

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